REMARKS

Claim Rejections Under 35 U.S.C. § 102

Claims 1-3 were rejected under 35 U.S.C. § 102(b) as being anticipated by *Le et al.* (U.S. Patent No. 5,727,005). Applicants respectfully traverse this rejection.

Claims 1, 5, 6, and 8 have been amended to include a limitation that a write operation is authorized if a protect status bit is in a first state or a security voltage is higher than a certain level. This limitation is found in the specification at paragraph 87. Therefore, no new matter has been added by this amendment.

Claims 2 and 4 have been amended to comply with antecedent basis requirements. A new claim 10 has been added that includes additional subject matter not yet claimed by Applicants. This subject matter is taught in the specification at paragraph 87 so that no new matter has been added by this amendment.

Le et al. disclose an integrated circuit microprocessor that accesses external memory. The external memory includes memory having a boot address. *Le et al.*, however, neither teach nor suggest Applicants' invention as claimed in the amended claims for a protection scheme in a system having multiple boot areas. *Le et al.* neither teaches nor suggests using a high voltage as a security voltage for the boot areas and not allowing access if the voltage is not high enough. Additionally, *Le et al.* neither teaches nor suggests using more than one boot block of a plurality of boot blocks if one boot block does not have the required capacity.

Claim Rejections Under 35 U.S.C. § 103

Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Le et al.* in view of *Kynett et al.* (U.S. Patent No. 5,249,158). Claims 8-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Le et al.* in view of *Johnson et al.* (U.S. Patent No. 5,343,437). Claim 1-3, 5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ogura et al.* (U.S. Patent No. 5,991,197). Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ogura et al.* in view of *Kynett et al.* (U.S. Patent No. 5,249,158). Claims 6-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ogura et al.* in view of *Johnson et al.* Applicants respectfully traverse these rejections.

Kynett et al. disclose a flash memory blocking architecture. The memory in *Kynett et al.* has a boot block on either end of the memory addresses. *Kynett et al.*, however, neither teach nor

suggest using both a protect status bit and a security voltage as claimed in Applicants' amended claims.

Ogura et al. disclose a semiconductor memory device that has a boot block. *Ogura et al.*, however, neither teach nor suggest Applicants' invention, as claimed in the amended claims, of using a protect status bit and a security voltage to limit access to two boot blocks in memory.

Johnson et al. disclose a memory having nonvolatile and volatile memory arrays. *Johnson et al.*, however, neither teach nor suggest Applicants' invention as claimed in the amended claims, using a protect status bit and a security voltage to limit access to two boot blocks.

Even if it were obvious to combine the above-cited references, and Applicants maintain that it is not, no combination of any of the references would yield Applicants' invention as claimed in the amended claims.

CONCLUSION

For the above-cited reasons, Applicant respectfully requests that the Examiner allow the claims of the present application. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and no additional fee is required by this amendment and response.

Respectfully submitted,

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